Implementation of 8 Bit Series and Parallel Comparator using Reversible Logic Gate

Anisha Patel

Department of Electronics &Instrumentation, SVCE Indore

anishap209@gmail.com

***Abstract*—-** *Investigation on reversible logic expand impetus in the past decade due to its presentation in quantum computing and low power circuit implementation. Reversible circuits realized by the existing synthesis techniques are often sub-optimal and optimization methods are applied on them to reduce the 'cost', a metric used to equate reversible circuits. Quantum computers are the appropriate alternative to the classical systems. The objective of this work is to design a 8 bit series and parallel comparator using novel and efficient reversible logic gates like CNOT and TR.*

***Keywords*—** *CNOT Gate, TR Gate, Reversible Logic, Quantum Computing.*

I. INTRODUCTION

In current VLSI Technology, Consumption of has become a very important issue in consideration. Heat dissipation and power consumption and can be minimized by using reversible logic. It is very less in if we compare the power consumption of reversible logic circuits with irreversible logic circuits. The application of Reversible Logic is in Nano - technology, Quantum computing, Computer graphics, Optical computing, and Low Power VLSI etc . Ralf Launduer found that heat dissipation in irreversible circuits is not as of the procedure involved in the operation, but it is due to the bits that were erased during the logical computation process. He verified Launder's principle which describes the lower theoretical limit of heat dissipation in logical computation.

Launder's principle states that losing a single bit information in the circuit causes the smallest quantity of heat in the computation which is equal to KTln2 joules where K is Boltzmann constant (approximately 1.38×10-23 J/K), T is Temperature and ln2 is natural algorithm of 2 (approximately 0.69315). The amount of heat which is simple in circuits is very minute but it becomes large in the complex circuits. It is essential to observe that there was straight relationship between the numbers of information bits erased to the amount of heat dissipated in the circuit. Later in 1973 C. H. Bennett described that the power dissipation due to the bit loss can be overcome if all computation in circuit was carried out in reversible manner. Quantum networks are designed of quantum logic gates. As each gate executes a unitary operation, KTln2 Joules energy dissipation wouldn't happen if the computation is carried out in reversible manner. He argued that for zero heat dissipation, the computation must be done in reversible manner. But if reversible logic is utilized to do logical computation, the heat dissipation will be less than KTln2 for one information bit in contrast to Launder. Thus computation done in reversible manner doesn't require erasing of bits [1].

Moore's law state that in an integrated circuit the number of transistors that are integrated per square inch gets doubled every year. Current VLSI technology has already in Nanotechnology and researchers were expecting that the roadmap of Moore's law no more gets satisfied because the the transistor size can't be reduced more without falling into leakage problems. The logical voltages can't be reduced more than their current levels without compromising impacting power and consumption to efficiency. Reversible logic gives an attractive solution and there will be a probable way to improve performance if the information bits are conserved by un-computing than erasing them. Energy efficiency improved in logical reversible computing. Speed of the circuits affected by energy efficiency of logical reversibility. Although in reversible computing the hardware complexity increases, the of power consumption and cost of performance are dominating the logical cost of hardware. Hence the requirement of logical reversible computing cannot be ignored [2].

II. CONCEPT

The Reversible Logic make use of of Reversible gates which consists of the equal number of inputs and outputs i.e., If the device obey following two conditions, it satisfies the second law of thermodynamics which preserves the information bits without getting erased and guarantees that no heat is dissipated. There must be one to one mapping between input vector lines and output vector lines. And the reversible gates are ready to run both forward and backward directions.

Some limitations are to be considered when designing circuits which based on reversible logic [3]

i. Fan out is not permitted in reversible logic and

ii. Feedback is also not permitted in reversible logic.

We can obtain full knowledge of inputs in Reversible logic using outputs. Fan-out limitation can be overcome by using additional reversible combinational circuits, the output lines are duplicated into required number of lines that are required to drive the inputs of consecutive device. Delay elements are used for feedback limitation.

III. RELATED WORK

Figure 1 shows that the Reversible logic gate consists of equal number of inputs and outputs. The basic Reversible logic gates present in the literature are shown below. The gates that are suitable for the design with optimum quantum cost can be selected.

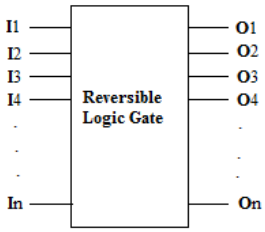


Figure 1: Simple reversible logic gate

The simplest Reversible gate is NOT gate and is a 1*1 gate. The example of a gate is 2*2 Controlled NOT (CNOT) gate. 3*3 Reversible gates are such as Toffoli gate, Feynman, Peres gate and Fredkin gate. The Quantum Cost of 1*1 Reversible gate and 2*2 Reversible gates are zero and one respectively. Any Reversible gate is realized by using 1*1 NOT gates and 2*2 Reversible gates, such as V, V+ (V is square root of NOT gate and V+ is its Hermitian) and FG gate which is also known as CNOT gate. The V and V+ Quantum gates have the property given in the Equations 1, 2 and 3 [4].

$$V * V = NOT \quad (1)$$
$$V * V+ = V+ * V = I \quad (2)$$
$$V+ * V+ = NOT \quad (3)$$

CNOT gate is also known as controlled-not gate. It is a 2*2 reversible gate. The CNOT gate can be described as:

Iv = (A, B);

Ov = (P= A, Q= A^B)

Iv and Ov are input and output vectors respectively. Quantum cost of CNOT gate is 1.

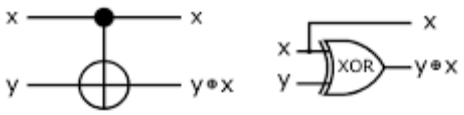


Figure 2: CNOT gate

TR gate is a 3*3 reversible gate. The TR gate can be described as:

Iv = (A, B, C);

Ov = (P= A, Q= A xor B, R= AB' xor C)

Iv and Ov are input and output vectors respectively. Quantum cost of TR gate is 6.

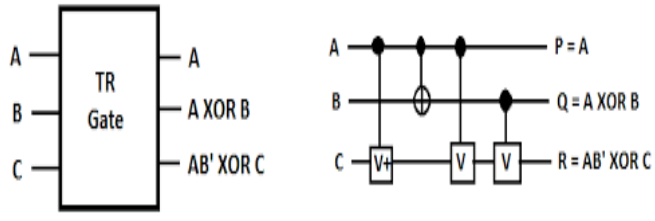


Figure 3: TR gate

The proposed design is realized by cascading three stages. The first stage is a 1-bit reversible comparator which generates 'greater' and 'equal' signals of that operand bit. These signals are combined using prefix tree grouping logic to generate final 'greater' and 'equal' signals. Using these final 'greater' and 'equal' signals, 'lesser' signal is generated in the third stage. The design is optimized in quantum level for efficient performance in all the cost metrics**.** The proposed comparator design results in reduced quantum delay reduced quantum cost and reduced garbage outputs when compared with the best existing design of prefix based comparator. Because here we are designing this by combining tree based and prefix based design [5].

IV. Methodology

The input circuit to binary comparator using reversible logic is shown in Figure 4. This circuit consists of three inputs An, Bn and logical low i.e., 0 and the outputs A Equal to B (AEB), A Greater than B (AGB) and A Less than B (ALB). The reversible input circuit is designed using one PG, two CNOT and one NOT gates.

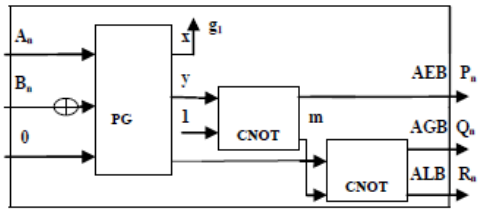


Figure 4: Proposed Reversible Binary Comparator

Eight-bit reversible binary comparator is shown in Figure 5. First stage is input circuit stage compares the MSB bits of the two numbers A8, B8. Second stage is one-bit comparator cell compares the result of the first stage and the input bits A7, B7 and so on. The final stage compares the output of the seventh stage and the LSB bits A1, B1 resulting the final output of the eight-bit numbers A and B.

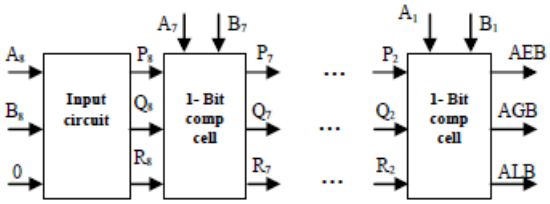
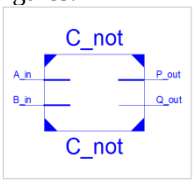


Figure 5: 8 bit reversible comparator

V. Simulation and Results

Reversible 2 bit and 8 bit comparator using TR gate and CNOT gate are implemented using VHDL code and Simulated using ISim Simulator. The individual gate functionality is implemented using Behavioral style of Modeling; the overall logic is implemented using Structural style of Modeling and simulation results are shown in following figures:



(a)

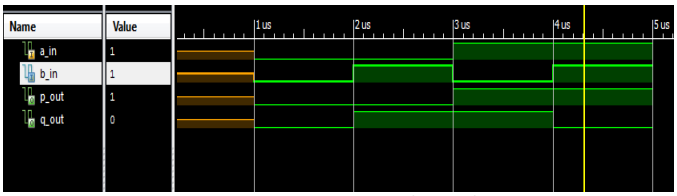
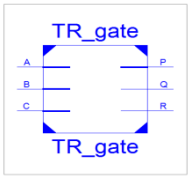


Figure 6: (a) RTL view, (b) Output waveform of CNOT gate



(a)

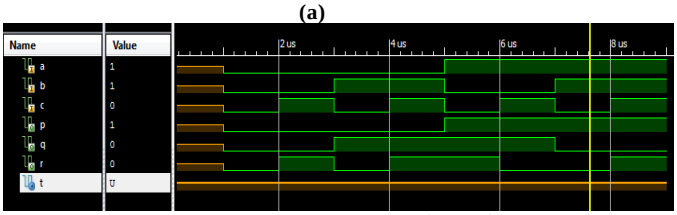


Figure 7: (a) RTL view, (b) Output waveform of TR gate

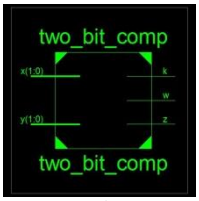


Figure 8: RTL view of two bit comparator

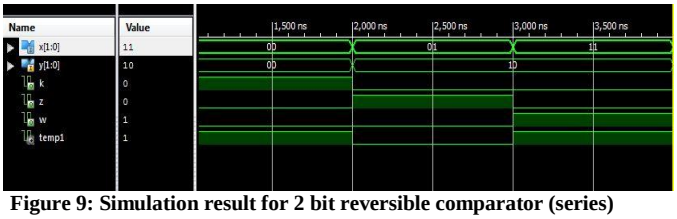


Figure 9: Simulation result for 2 bit reversible comparator (series)

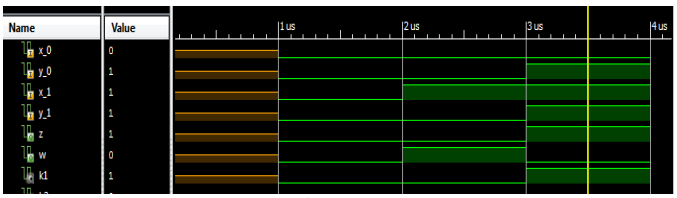


Figure 10: Simulation result for 2 bit reversible comparator (parallel)

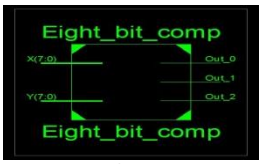


Figure 11: RTL view of 8 bit comparator (series)

Figure 12: Simulation result for 8 bit reversible comparator (series)

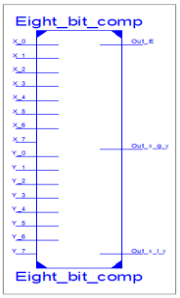


Figure 13: RTL view of 8 bit comparator (parallel)

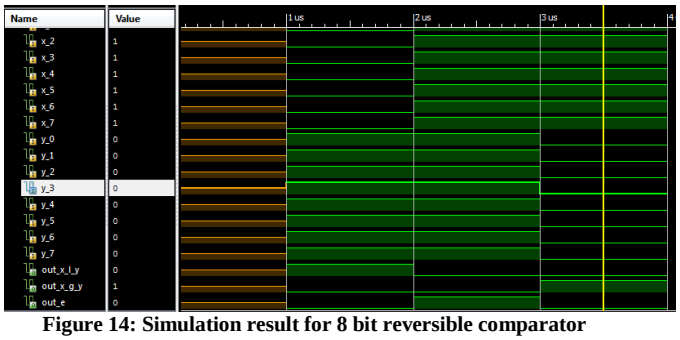


Figure 14: Simulation result for 8 bit reversible comparator (parallel)

Table 1: Device utilization summary for reversible gate

S.No	GATE	QC	Delay (ns)	Memory (KB)
1	CNOT	1	5.259	179080
2	TR	6	5.385	179848

Table 2: Device utilization summary for reversible comparator

S.No	Slice Logic Utilization	TR GATE & CNOT GATE			
		Series		Parallel	
		2	8	2	8
1	Number of Slice LUTs	10	49	1	7
2	Number of occupied Slices	4	23	1	4
3	Number of bonded IOBs	19	100	6	17
4	Delay (nSec)	8.509	10.804	5.439	8.05
5	Total memory usage (KB)	209668	182664	181000	195336
6	Quantum Cost	13	91	13	91

Table 3: Comparison of existing and proposed designs

S. No	Comparator	Tree based Design	Design [6]	Proposed Design
1	8-bit	135	135	91

VI. CONCLUSIONS

The reversible logic design helps to improve heat and power management. The potential area of reversible logic design is in the field of quantum computer, optical computing and bio molecular computations. These are the basic building block of quantum computers. The implemented design shows the quantum cost and delay in the output.

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